ELECTION OF CLAIMS

The Examiner has required restriction to one of the following groups of claims:

Group I: Claims 1-2 and 12, drawn to a method of delay change determination/aligning aggressor signals associating with nominal and noisy victim net signal transition arrival time/waveforms, classified in class 716, subclass 06.

Group II: Claims 3-6, drawn to a method of determining aggressor-induced delay change with voltage dependent current model and interconnect model, classified in class 703, subclass 19.

Group III: Claims 7-11, drawn to a method of determining aggressor-induced delay change with using a computation model and pre-computed aggressor waveform, classified in class 703, subclass 02.

Applicants hereby elect Group II as defined by the Examiner, specifically Claims 3-6, without traverse.

AMENDMENTS TO THE CLAIMS

1. (withdrawn) A method of delay change determination in an integrated circuit design including a stage with a victim net and one or more aggressor nets capacitively coupled thereto, the method comprising:

determining a nominal victim net signal transition arrival time at an output of a victim net receiver;

determining a noisy victim net signal transition arrival time at the output of the victim net receiver, wherein the noise is due to one or more aggressors; and

determining a delay change based upon nominal and noisy victim signal transition arrival times at the receiver output.

2. (withdrawn) A method of delay change determination in an integrated circuit design including a stage with a victim net and one or more aggressor nets capacitively coupled thereto in an interconnect network, the method comprising:

(1) determining a nominal (noiseless) victim net signal transition using a method including the steps of,

providing a nominal victim signal transition waveform on a victim driver output based on a signal transition on the victim driver input;

propagating the nominal victim signal transition waveform from the victim driver output to a victim receiver input via the interconnect network; and

further propagating the nominal victim signal transition waveform from the victim receiver input to a victim receiver output;

(2) determining a noisy victim net signal transition using a method including the steps of,

providing a noisy victim signal transition waveform on the victim driver output based on the signal transition on the victim driver input and an aggressor-induced current waveform;

propagating the computed victim driver output waveform from the victim driver output to the victim receiver input via the interconnect network so as to produce a propagated victim voltage waveform at the victim receiver input; and

providing an aggressor-induced voltage waveform to the victim receiver input;

computing a noisy victim receiver input voltage waveform using the propagated victim voltage waveform and the aggressor-induced voltage waveform; and

propagating the noisy victim receiver input voltage waveform from the victim receiver input to the victim receiver output; and

(3) determining a delay change based upon nominal and noisy victim signal transition arrival times at the receiver output.

3. (original) A method of determining aggressor-induced delay change in a victim net of a stage of an integrated circuit design, comprising:

providing an input and output voltage dependent current model of a driver of the victim net;

producing a model of an interconnect network of the stage, which can be used to propagate a waveform from an output of the driver model to an input of a victim net receiver;

determining nominal (noiseless) delay in the stage by determining delay associated with the steps of,

providing a signal transition to the driver model;

using the interconnect model to propagate a driver model output waveform, resulting from the provided signal transition, from the driver model output to the receiver input;

determining noisy delay in the stage by determining delay associated with the steps of,

providing a signal transition to the driver model;

providing at least one aggressor-induced current waveform to an output of the driver model;

using the interconnect model to propagate a driver model output waveform, resulting from the provided signal transition and from the at least one aggressor-induced waveform, from the driver model output to the receiver input;

providing at least one aggressor-induced voltage waveform to an input of the receiver; and

determining a difference between the nominal delay and noisy delay.

4. (original) The method of claim 3,

wherein the output current-dependent model of a driver of the victim net includes a ViVo model.

5. (currently amended) The method of claim 3,

wherein the output current-dependent model of a driver of the victim net includes a ViVo model; and

wherein the interconnect model includes a Π-load.

6. (currently amended) The method of claim 3,

wherein determining nominal delay further includes propagating the propagated driver model output waveform to an output of the receiver; and

wherein determining noisy delay in the stage includes propagating the propagated driver output waveform and the provided at least one aggressor induced waveform to an output of the receiver.

7. (withdrawn) A method of producing an aggressor-induced victim net waveform, for use with an integrated circuit design that includes a stage with a victim net capacitively coupled to one or more aggressor nets through an interconnect network, a victim net driver and a victim net receiver, the method comprising the steps of:

producing a computational model of the interconnect network, which model can be used to compute a victim net waveform from an aggressor net waveform; and

inputting the aggressor net waveform to the computational model.

8. (withdrawn) A method of producing an aggressor-induced victim net waveform, for use with an integrated circuit design that includes a stage with a victim net capacitively coupled to one or more aggressor nets through an interconnect network, a victim net driver and a victim net receiver, the method comprising the steps of:

producing a computational model of the interconnect network, which model can be used to compute a victim net waveform form an aggressor net waveform;

pre-computing an aggressor waveform corresponding to a prescribed aggressor signal transition on at least one aggressor net, which takes account of the influence of at least one other net capacitively coupled to the at least one aggressor net; and

inputting the pre-computed aggressor waveform to the computational model.

9. (withdrawn) The method of claim 8,

wherein the prescribed aggressor signal transition is a fastest aggressor net signal transition.

10. (withdrawn) A computer readable medium encoded with a waveform produced by the method of claim 8.

11. (withdrawn) A computer readable medium encoded with a waveform produced by the method of claim 9.

12. (withdrawn) A method of aligning one or more aggressor signals with a victim signal transition for use with an integrated circuit design that includes a stage, with a victim net capacitively coupled to one or more aggressor nets through an interconnect network, a victim net driver and a victim net receiver, the method comprising the steps of:

providing at least one aggressor induced victim net waveform associated with an aggressor net, wherein the at least one provided waveform is induced in the victim net by a prescribed aggressor signal in the associated aggressor net;

determining respective delays associated with a victim net signal transition from the victim driver to the victim receiver, while the at least one aggressor induced victim net waveform is imparted to the victim net, for each of multiple alignments of the at least one provided waveform with the victim net signal transition;

interpolating a next alignment of the victim net signal transition and the at least one provided waveform based upon previously determined delays, wherein the next alignment is selected to result in a worse delay than prior alignments;

determining a respective next delay associated with the next alignment;

repeating the interpolating step and the determining a respective next delay step until a prescribed limit is reached.

13. (new) A model of a gate circuit comprising:

a current model that associates instantaneous values of input node voltage, output node voltage and output node current of the gate circuit;

a model of capacitance between an input node and an output node of the gate circuit; and

a model of capacitance between the output node of the gate circuit and a ground potential.

14. (new) The model of claim 13 wherein,

the gate circuit current model includes a model of at least one channel connected component of the gate circuit.

15. (new) The model of claim 13 wherein,

the gate circuit current model includes a model of a last channel connected component of the gate circuit.

16. (new) The model of claim 13 wherein,

the gate circuit current model includes only a model of a last channel connected component of the gate circuit.

17. (new) The model of claim 13, further including:

information concerning slew rate on the input node of the at least one component characterized as a function of slew rate on at least one input node of the gate.

18. (new) The model of claim 13,

wherein the gate circuit current model includes only a model of a last channel connected component of the gate circuit; and further including:

information concerning slew rate on the input node of the at least one component characterized as a function of slew rate on at least one input node of the gate.

19. (new) A model of a gate circuit comprising:

a current model that associates instantaneous values of gate circuit input node voltage, gate circuit output node voltage and gate circuit output node current;

a model of miller capacitance of the output node of the gate circuit; and

a model of ground capacitance of the output node of the gate circuit.

20. (new) The model of claim 19 further including:

information concerning slew rate on the input node of the at least one component characterized as a function of slew rate on at least one input node of the gate.

21. (new) A circuit simulation process to produce a current model of a gate circuit comprising:

for each of a plurality of different pairs of first and second DC voltage values,

sensitizing an input node of a cell model of the gate circuit with a first DC voltage value; and

sensitizing an output node of the cell model with a second DC voltage value; and

generating a value of current drawn by the output node of the cell model based upon the provided first DC voltage value and the provided second DC voltage value.

22. (new) The method of claim 21 further including:

producing a table representing respective associations among respective pairs of first DC voltage values and second DC voltage values and respective current values generated based upon such respective pairs.

23. (new) The method of claim 21 wherein,

each respective first DC value includes a constant DC value; and

each respective second DC value includes a constant DC value.

24. (new) The method of claim 21 wherein,

the gate circuit model includes a model of at least one channel connected component of the gate circuit.

25. (new) The method of claim 21 wherein,

the gate circuit model includes a model of a last channel connected component of the gate.

26. (new) The method of claim 21 wherein,

the gate circuit model includes only a model of a last channel connected component of the gate.

27. (new) The method of claim 21, further including:

producing a model of capacitance between the input node of the and the output node of the gate circuit; and

producing a model of capacitance between the output node of the gate circuit and a ground potential.

28. (new) The method of claim 21, further including:

determining capacitance between the input node and the output node of the gate circuit through transient analysis; and

determining capacitance between the output node the gate circuit and a ground potential through transient analysis.

29. (new) The method of claim 31, further including:

determining a slew rate on an input node of the cell model of the gate circuit characterized as a function of slew rate on an input node of the cell model of the gate circuit.

30. (new) The method of claim 31,

wherein the gate circuit model includes only a model of a last channel connected component of the gate; further including:

determining a slew rate on an input node of the cell model characterized as a function of slew rate on an input node of the cell model of the gate circuit.

31. (new) An article of manufacture including a computer readable medium encoded with a data structure representing a current model of a gate circuit, the data structure associating input voltage values, output voltage values and current values, the data structure produced by a process including the steps of:

for each of a plurality of different pairs of first and second DC voltage values,

sensitizing an input node of a cell model representing the gate circuit with a first DC voltage value; and

sensitizing an output node of the cell model with a second DC voltage value; and

generating a value of current drawn by the output node of the cell model based upon the provided first DC voltage value and the provided second DC voltage value.

32. (new) The article of claim 31 wherein the process further includes the step of:

producing a table representing the respective associations among first DC voltage values, second DC voltage values and current values.

33. (new) The article of claim 31 wherein,

each respective first DC value includes a constant DC value; and

each respective second DC value includes a constant DC value.

34. (new) A method of simulating aggressor-induced behavior of a gate circuit and an interconnect network driven by the gate circuit, comprising:

providing a voltage signal transition on an input of a current model representing the gate circuit, the current model associating instantaneous values of input voltage, output voltage and output current of the gate circuit;

providing an aggressor induced current waveform on a node interconnecting an output of the current model and a load model representing the interconnect network, the load model approximating output point admittance of the interconnect network; and

using the current model and the load model to produce a voltage waveform on the output of the current model based upon the received input voltage signal transition and the received aggressor induced waveform.

35. (new) The method of claim 34,

wherein the current model includes a model of capacitance of the at least one component.

36. (new) The method of claim 34,

wherein the current model includes a model of miller capacitance of the at least one component; and

wherein the current model includes a model of gate capacitance of the at least one component.

37. (new) The method of claim 34 wherein,

the load model includes a Π-model.

38. (new) The method of claim 34 wherein,

the at least one component comprises a channel connected component.

39. (new) The model of claim 34 wherein,

the current model includes a model of a last channel connected component of the gate.

40. (new) A method of simulating aggressor-induced delay change in a victim net in an integrated circuit design, the victim net including a driver circuit, a receiver circuit and an interconnect network between the driver circuit and the receiver circuit, the method comprising:

determining nominal (noiseless) delay in the victim net by determining delay associated with a signal propagation process comprising,

providing a voltage signal transition on an input of a current model of the driver circuit in which a node interconnects an output of the current model and a load model representing the interconnect network, the load model approximating output point admittance of the interconnect network, so as to produce a current model nominal output voltage waveform; and

using a computational model of the interconnect network to propagate a voltage waveform to an input of a model of the receiver in response to the current model nominal output voltage waveform;

determining noisy delay in the victim net by determining delay associated with a signal propagation process comprising,

providing a voltage signal transition on the input of the current model of the driver circuit and providing an aggressor induced current waveform to the output node of the current model that interconnects the output of the current model and the load model representing the interconnect network, so as to produce a current model noisy output voltage waveform; and

using the computational model of the interconnect network to propagate a voltage waveform to an input of a model of the receiver in response to the current model noisy output voltage waveform; and

determining a difference between the nominal delay and noisy delay.

41. (new) The method of claim 40,

wherein the current model includes a model of capacitance of the driver circuit.

42. (new) The method of claim 40,

wherein the current model includes a model of miller capacitance of the driver circuit; and

wherein the current model includes a model of gate capacitance of the driver circuit.

43. (new) The method of claim 40 wherein,

the load model includes a Π-model.

44. (new) The method of claim 40 wherein,

the current model includes a model of a last channel connected component of the driver circuit.

45. (new) The method of claim 40 wherein,

the computational model of the interconnect network includes one or more transfer functions that relate a signal on a driver circuit output node to a signal on a receiver circuit input node.

46. (new) The method of claim 40 wherein,

the model of the receiver includes a current model.

48. (new) The method of claim 40 wherein,

the driver circuit current model associates instantaneous values of input node voltage, output node voltage and output node current of the gate circuit.

49. (new) The method of claim 40 wherein,

the driver circuit current model associates instantaneous values of input node voltage, output node voltage and output node current of the gate circuit; and

the driver circuit current model includes a model of capacitance between an input node and an output node of the gate circuit; and

the driver circuit current model includes a model of capacitance between the output node of the gate circuit and a ground potential.